

I2S bus Timing Test Report

Project code	HW Version	SW Version	
K18X001T00	V125	19.522.17-20210422	
Tester	Tom lee	Test date	2021/06/03

1.1 Test Steps

1.1.1 Connect main board and sub-board as environment

1.1.2 Power on DUT

1.1.3 Connect J806 (AUX IN) to mobile phone, then mobile plays YouTube video.

1.1.4 Input below commands

adb connect 192.168.2.102:5815 (192.168.2.102 is DUT IP)

setup.bat 192.168.2.102 192.168.2.100

(192.168.2.102 is DUT IP, 192.168.2.100 is iPerf server IP)

1.1.5 When the speaker sounds, then start to measure I2S wave.

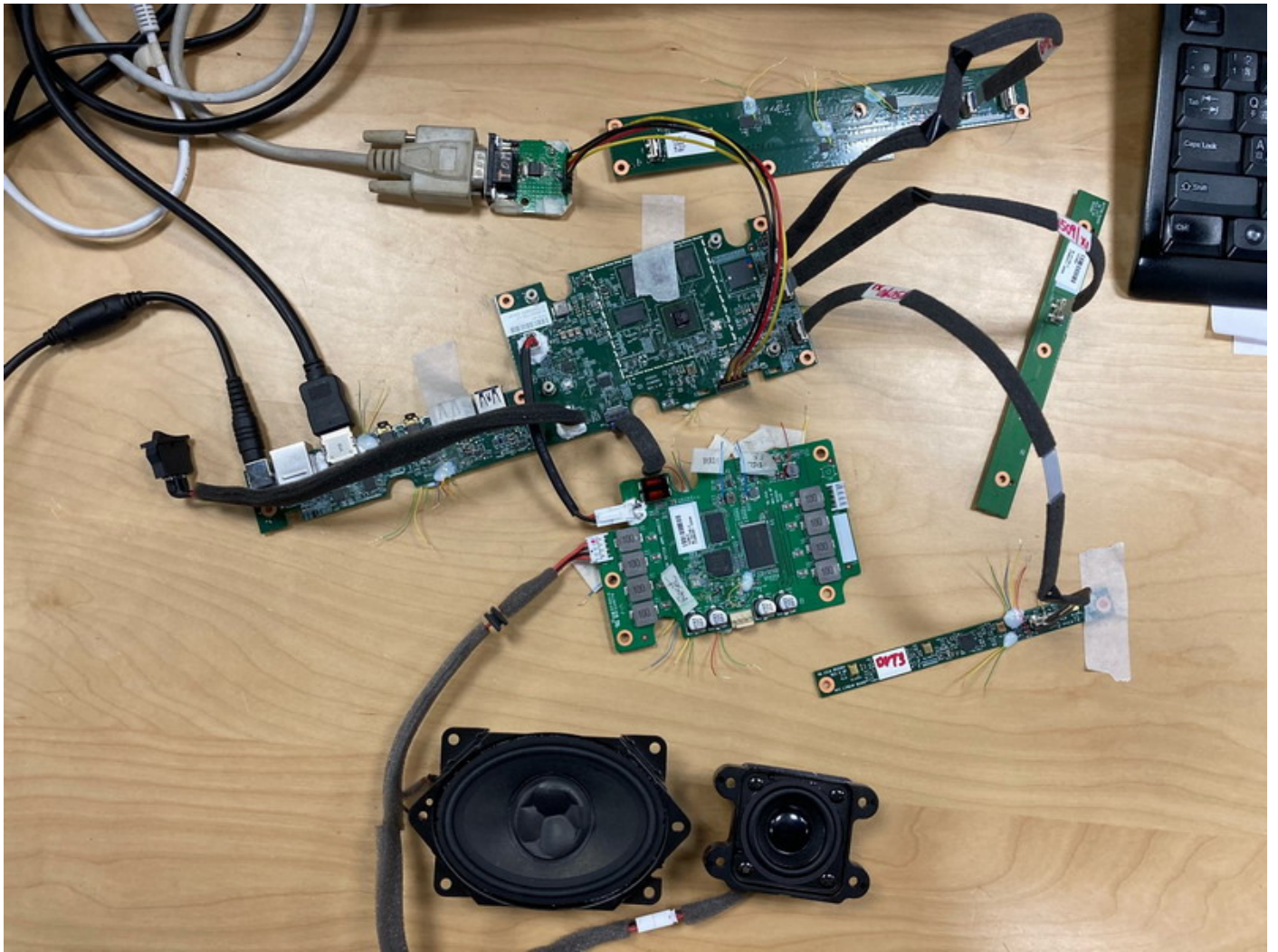
1.1.6 Measurement point.

A113X Input: BCLK: 5R68, LRCK: 5R67, Data: 5R69.

AMP IC: BCLK: TP309, LRCK: TP307, Data0 (Woofer): R225 pin2, Data1 (Full range): R231 pin 1.

ADC3100: BCLK: R2946, LRCK: R2947, Data: R2948.

CX20810: BCLK: R6_17, LRCK: R6_19, Data: R6_18.



Environment Picture

1.2 Specification

1.2.1 A113X Input

Figure 18 I2S/TDM Timing Diagram, Slave Mode

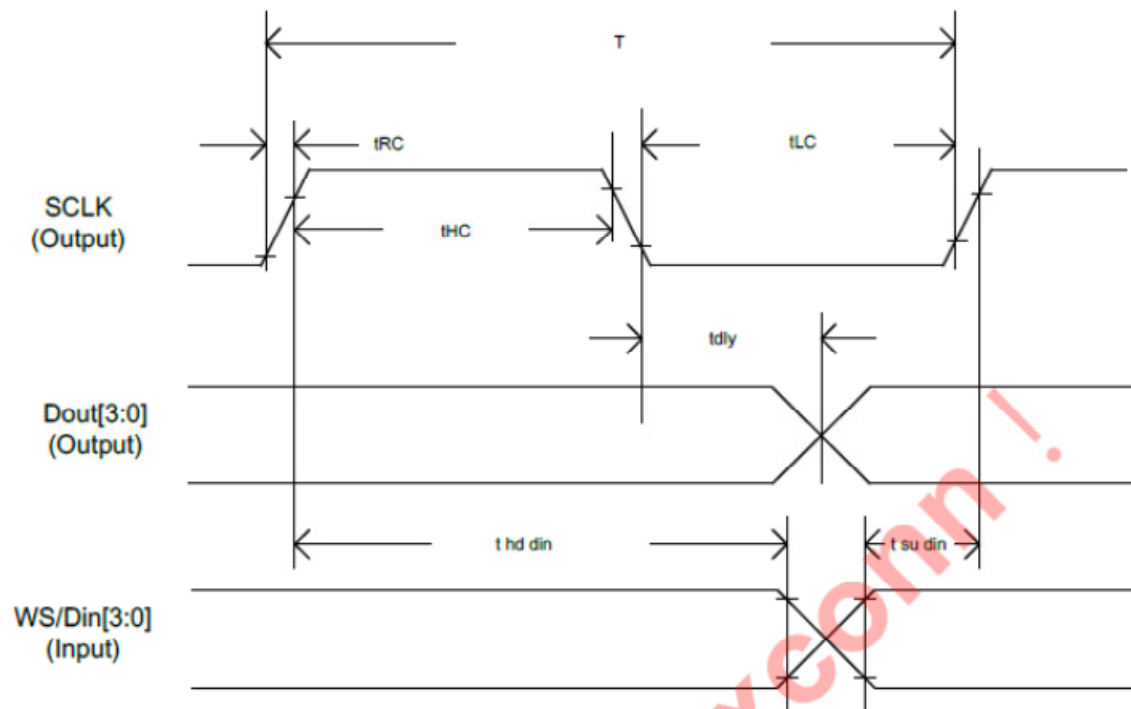


Table 34 Audio I2S/TDM Timing Specification, Transmitter, Slave Mode

Transmitter (slave mode)					
Symbol	Parameter	Min	Typ	Max	unit
T(out)	Clock period	40			ns
T(in)	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.8	ns
tsu in	Setup time of WS/Din	4			ns
thd in	Hold time of WS/Din	4			ns
tdly	Delay between SCLK and Dout	2	7	10	ns

9. Electrical Characteristics (Continued)

$T_A = 25^\circ\text{C}$, $V_{DDIO} = 3.3\text{V}$, $PVDDXX = 24\text{V}$, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
I²S Audio Interface						
BCK high time	t_{BH}		20		-	ns
BCK low time	t_{BL}		20		-	ns
SDATA setup time before BCK rising edge	t_{DS}		10		-	ns
SDATA hold time after BCK rising edge	t_{DH}		10		-	ns
WCK setup time before BCK rising edge	t_{WS}		20		-	ns
BCK rising edge before WCK edge	t_{WH}		20		-	ns

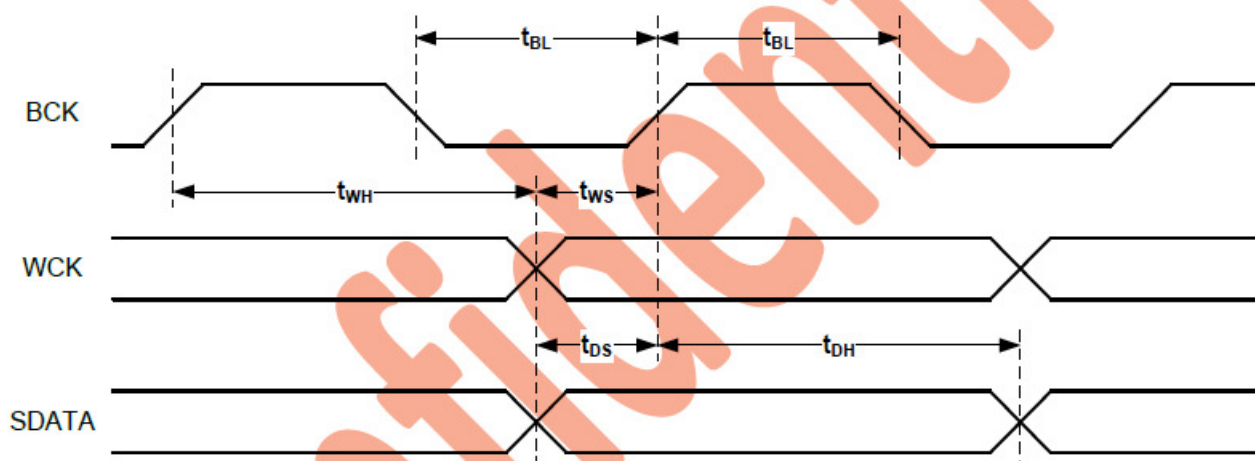


Figure 2. I²S Audio Interface Timing Diagram

1.2.3 Audio ADC TLV320ADC3100

7.8 Timing Requirements: I²S, LJF, RJF Timing in Slave Mode

specified at 25°C, DVDD = 1.8 V, all timing specifications are measured at characterization; see Figure 3 for a timing diagram

		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t _H (BCLK)	BCLK high period	35		35		ns
t _L (BCLK)	BCLK low period	35		35		ns
t _s (WS)	BCLK, WCLK setup time	10		6		ns
t _h (WS)	BCLK, WCLK hold time	10		6		ns
t _d (DO-WS)	BCLK, WCLK to DOUT delay time (for LJF mode only)		30		30	ns
t _d (DO-BCLK)	BCLK to DOUT delay time		25		20	ns
t _r	Rise time		16		8	ns
t _f	Fall time		16		8	ns

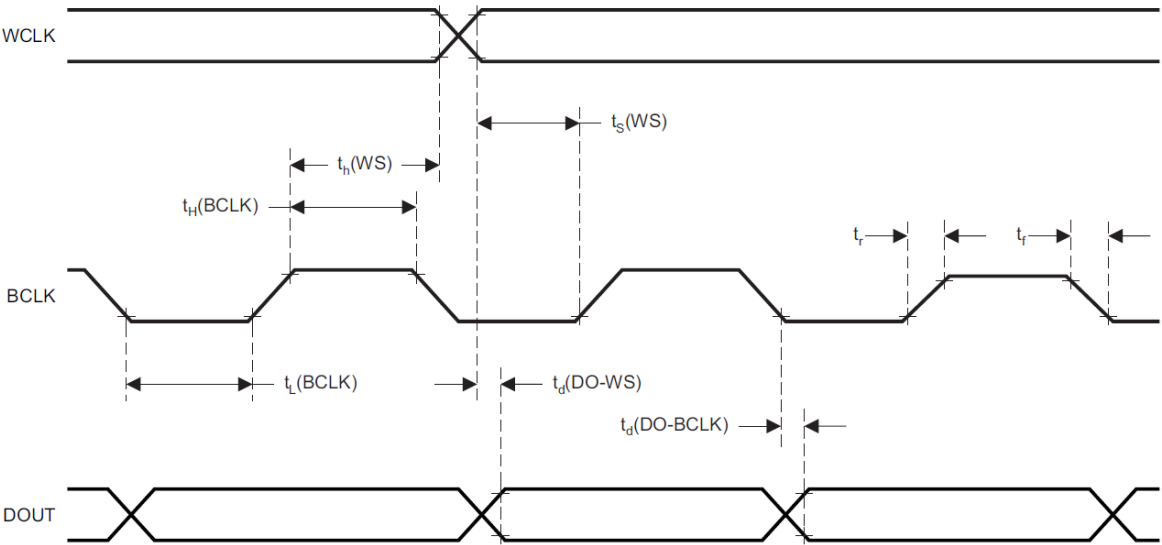


Figure 3. I²S, LJF, RJF Timing in Slave Mode

1.2.4 ADC CX20810

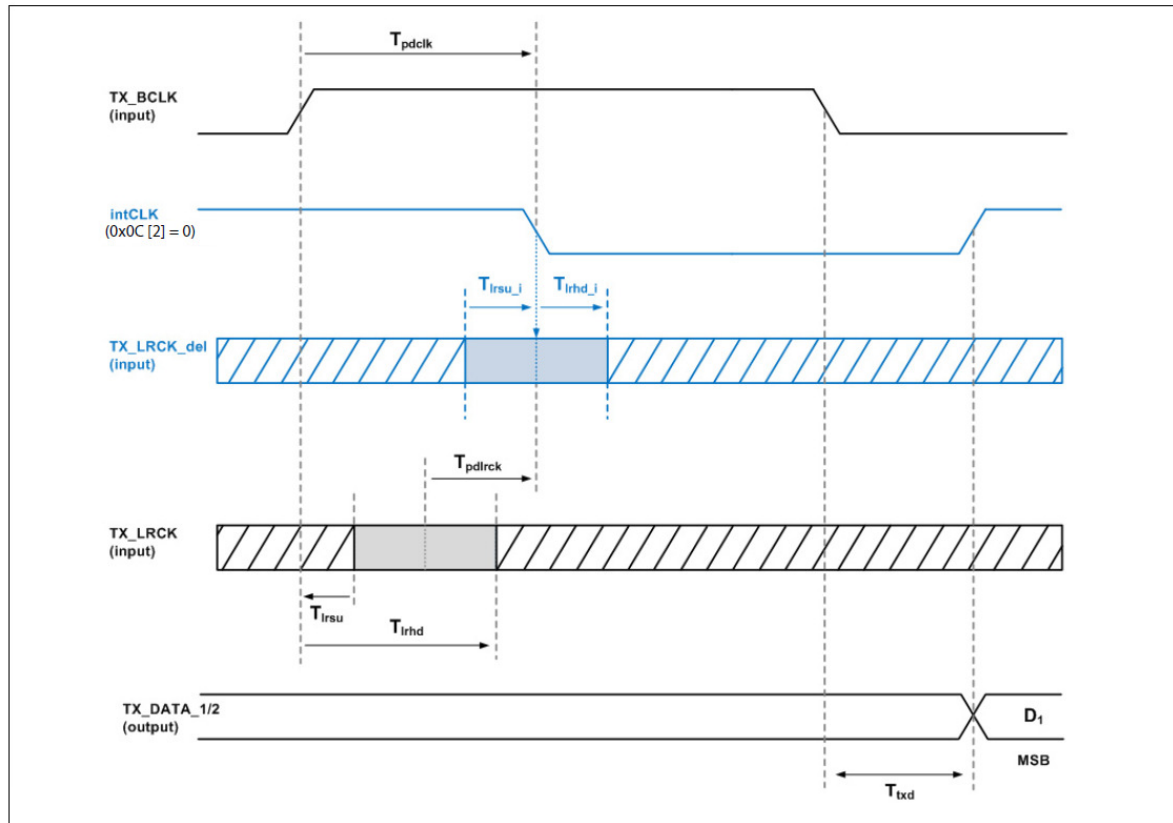


Figure 85: Slave Mode Timing Diagram: Data Transitions on Falling Edge of BCLK

- The BCLK and LRCK signals experience internal propagation delays due to pad and logic delays
- The internal logic setup and hold time requirements are less than 50 ps and are negligible relative to the propagation delay.
- Based on the worst case values, the minimum required setup time is -5 ns and minimum hold time is 7 ns. This is relative to the LRCK and BCLK signals seen at the device pins.
- Proper interface configuration will ensure around a half-cycle (~40 ns) of timing margin.

Table 114: Slave Mode Timing Specification

Parameter	Symbol	Min	Typ	Max	Unit
I2S/TDM bit clock cycle time	T_{CC}	80	81.38	–	ns
Internal propagation delay for TX_BCLK	T_{PDCLK}	10	–	12	ns
Internal propagation delay for TX_LRCK	T_{PDLRCK}	5	–	7	ns
TX_LRCK to TX_BCLK setup time	T_{LRSU}	-5	–	–	ns
TX_LRCK to TX_BCLK hold time	T_{LRHD}	+7	–	–	ns
TX Data propagation delay from falling edge of BCLK	T_{TXD}	5	–	20 *	ns

* Output delay assumes 3.3V IO and 30 pF load. For 1.8v IO and 20 pF load the max delay is 32 ns

1.3 Test Result

Chip	Parameter	Symbol	Min	Max	Unit	Result	Pass /Fail	Figure
A113X Input	Clock period	T(in)	10		ns	324.6	Pass	1
	High level of SCLK	tHC	0.4		T	0.492	Pass	2
	Low level of SCLK	tLC	0.4		T	0.497	Pass	3
	Edge time of SCLK	tRC		26	ns	3.135	Pass	4
	Setup time of WS	tsu in	4		ns	158.0	Pass	5
	Setup time of Din	tsu in	4		ns	162.8	Pass	6
	Hold time of WS	thd in	4		ns	164.1	Pass	7
	Hold time of Din	thd in	4		ns	162.1	Pass	8
AMP IC	BCK high time	tBH	20		ns	162.6	Pass	9
	BCK low time	tBL	20		ns	162.9	Pass	10
	SDATA setup time before BCK rising edge (Data 0)	tDS	10		ns	162.4	Pass	11
	SDATA hold time after BCK rising edge (Data 0)	tDH	10		ns	164.7	Pass	12
	SDATA setup time before BCK rising edge (Data 1)	tDS	10		ns	162.4	Pass	13
	SDATA hold time after BCK rising edge (Data 1)	tDH	10		ns	164.7	Pass	14
	WCK setup time before BCK rising edge	tWS	20		ns	0.065	Fail	15
	BCK rising edge before WCK edge	tWH	20		ns	324.9	Pass	16
TLV320 ADC3100	BCLK high period	tH(BCLK)	35		ns	163.1	Pass	17
	BCLK low period	tL(BCLK)	35		ns	161.8	Pass	18
	BCLK, WCLK setup time	ts(WS)	6		ns	158.5	Pass	19
	BCLK, WCLK hold time	th(WS)	6		ns	166.4	Pass	20
	BCLK to DOUT delay time	td(DO-BCLK)		20	ns	9.28	Pass	21
	Rise time	tr		8	ns	0.7	Pass	22
	Fall time	tf		8	ns	0.7	Pass	23
CX20810	TX_LRCK to TX_BCLK setup time	TLRSU	-5	-	ns	172.5	Pass	24
	TX_LRCK to TX_BCLK hold time	TLRHD	+7	-	ns	153.5	Pass	25
	TX Data propagation delay from falling edge of BCLK	TTXD	5	20	ns	15.8	Pass	26

1.4 Wave

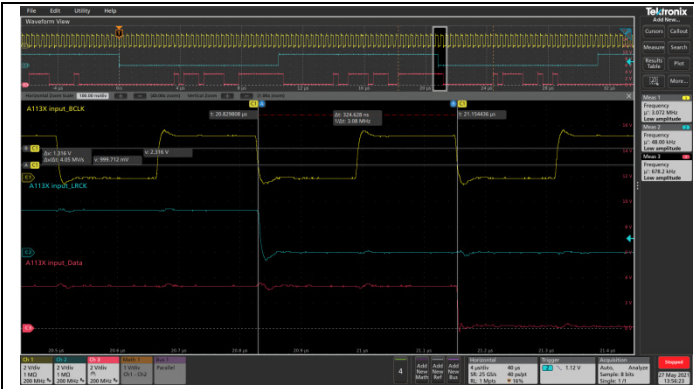


Figure 1: Clock period

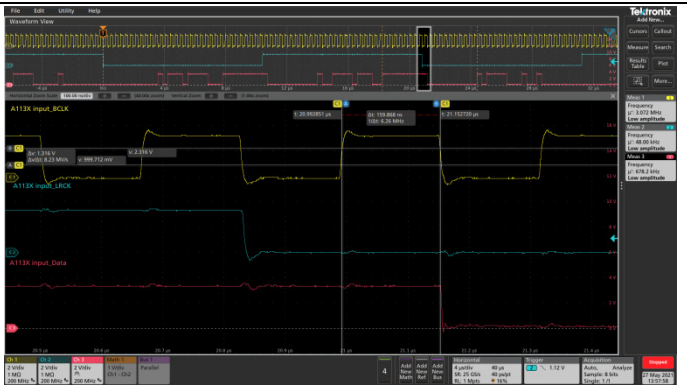


Figure 2: High level of SCLK

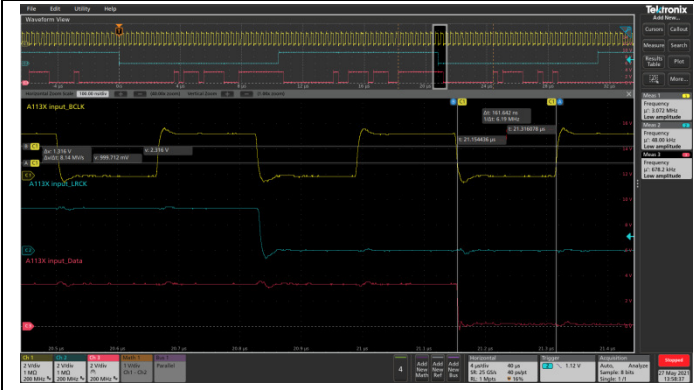


Figure 3: Low level of SCLK

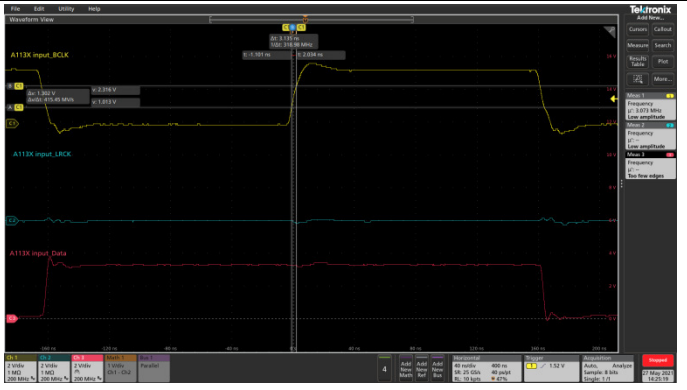


Figure 4: Edge time of SCLK

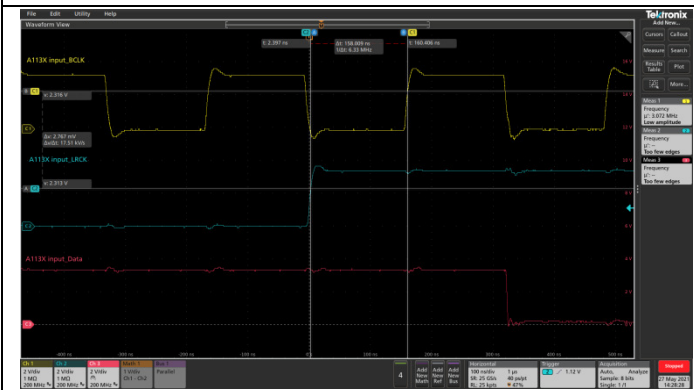


Figure 5: Setup time of WS

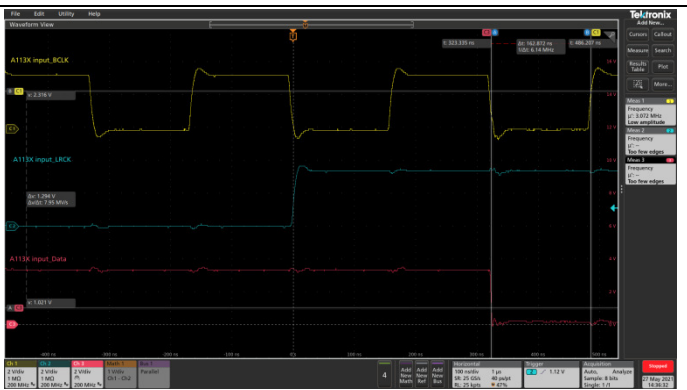


Figure 6: Setup time of Din

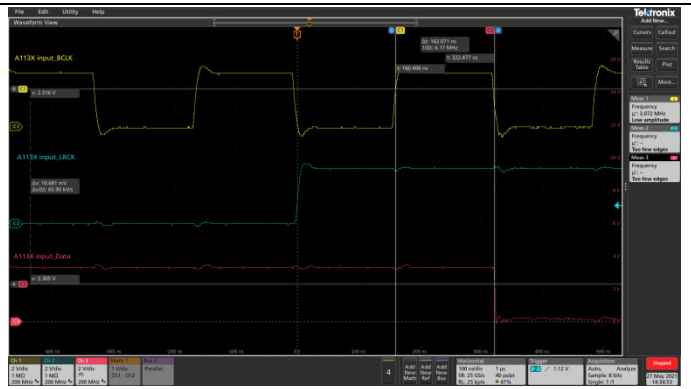
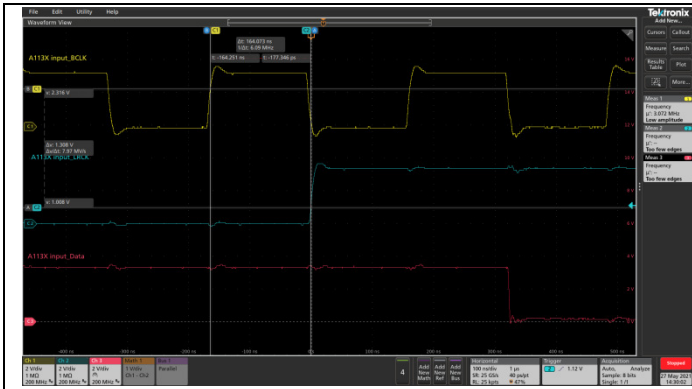


Figure 7: Hold time of WS

Figure 8: Hold time of Din

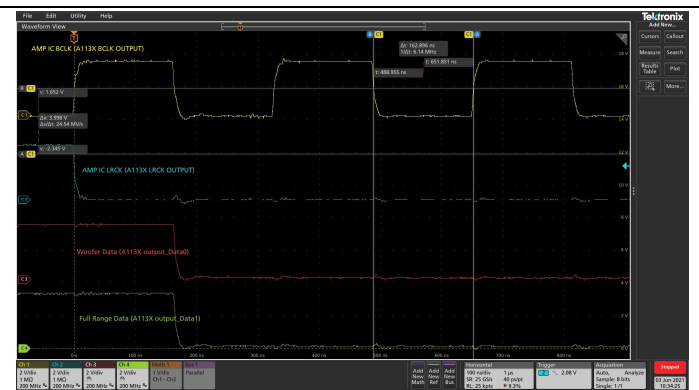
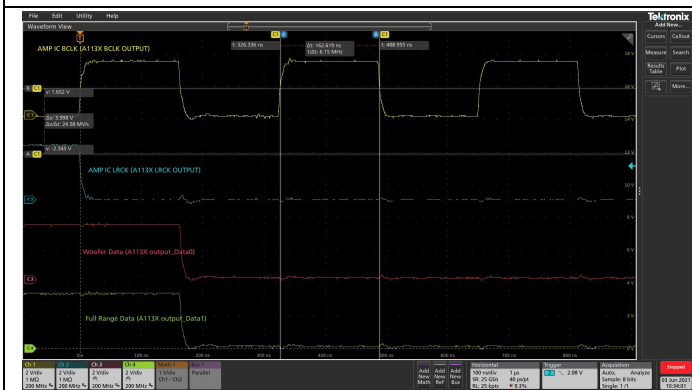


Figure 9: BCK high time

Figure 10: BCK low time

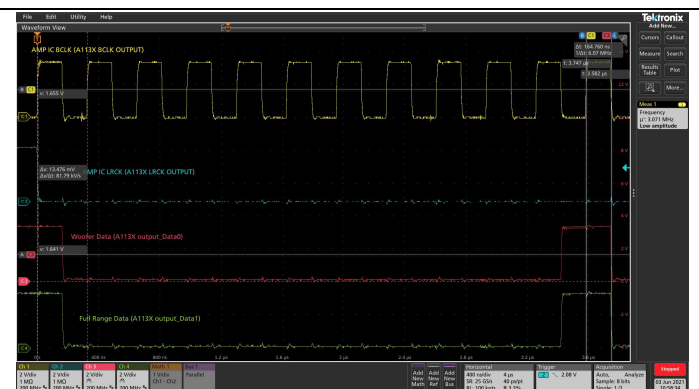
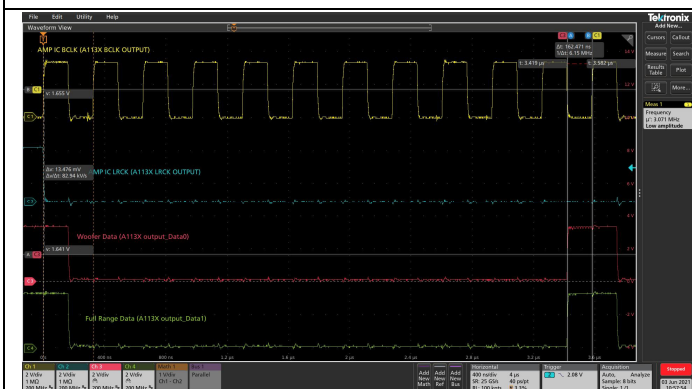


Figure 11: SDATA setup time before BCK rising edge (Data 0)

Figure 12: SDATA hold time after BCK rising edge (Data 0)

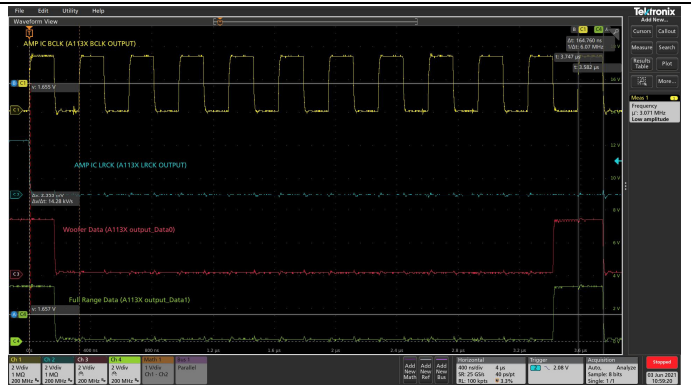
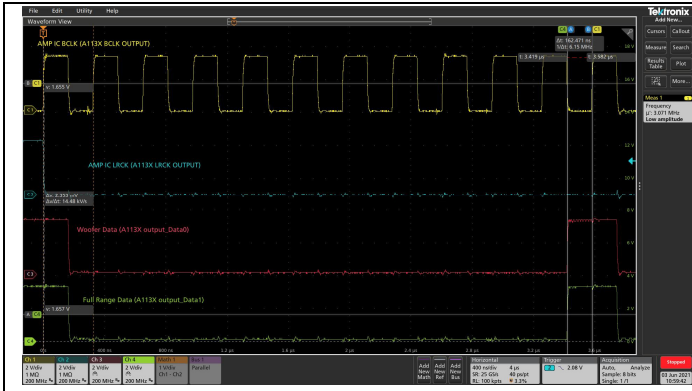


Figure 13: SDATA setup time before BCK rising edge (Data 1)

Figure 14: SDATA hold time after BCK rising edge (Data 1)



Figure 15: WCK setup time before BCK rising edge

Figure 16: BCK rising edge before WCK edge

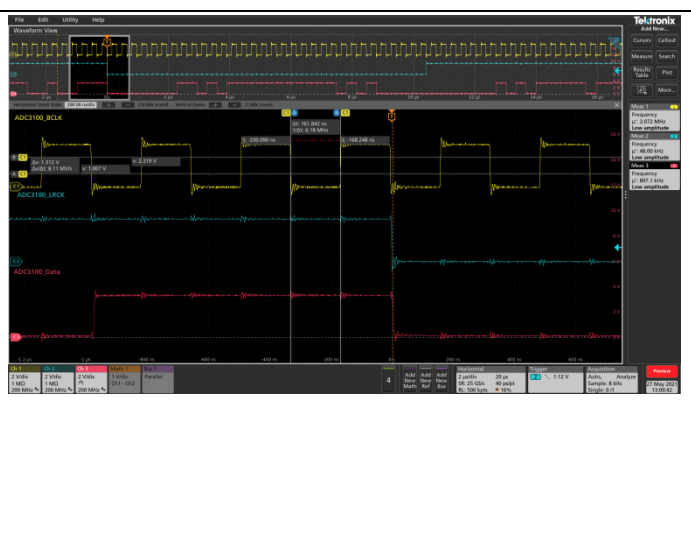
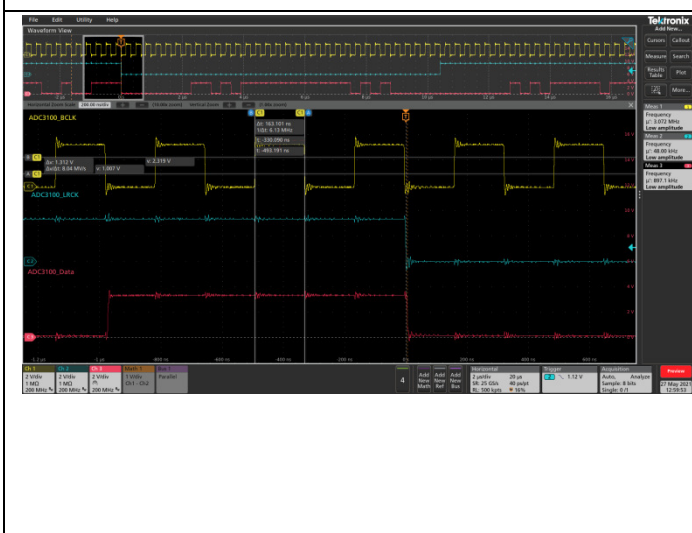


Figure 17: BCLK high period

Figure 18: BCLK low period

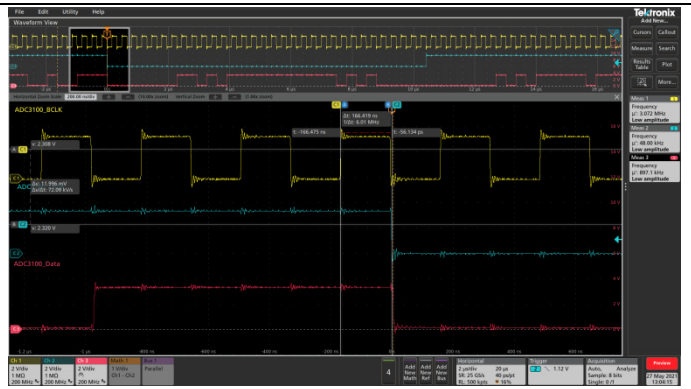
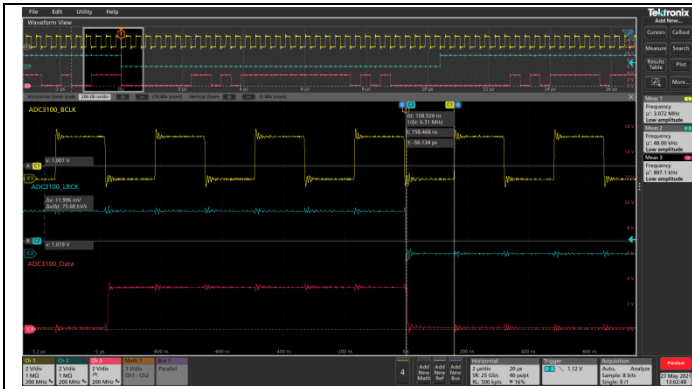


Figure 19: BCLK, WCLK setup time

Figure 20: BCLK, WCLK hold time

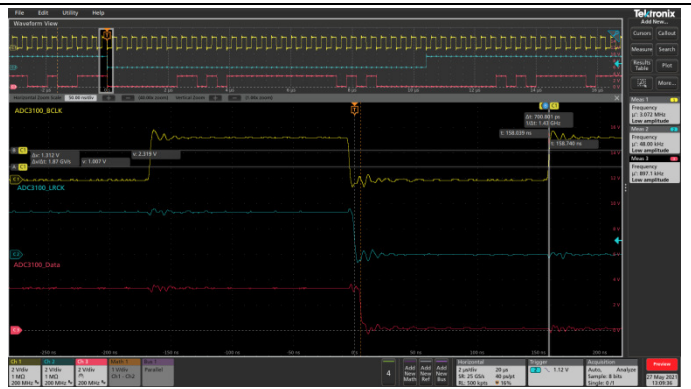
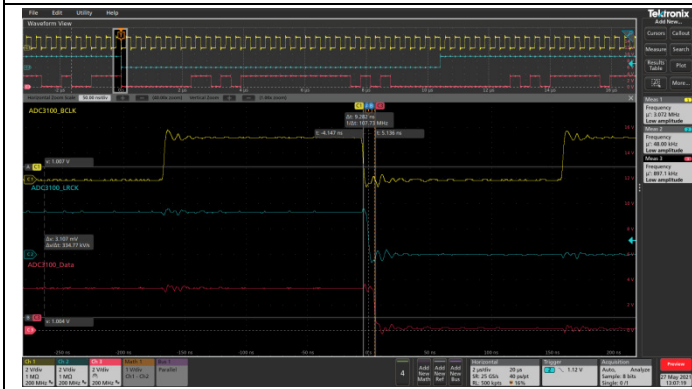


Figure 21 : BCLK to DOUT delay time

Figure 22: Rise time

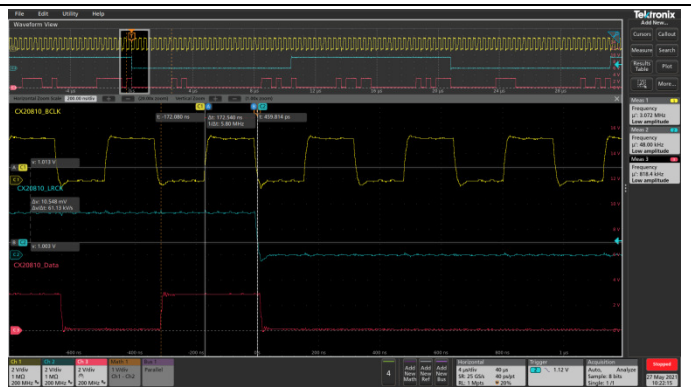
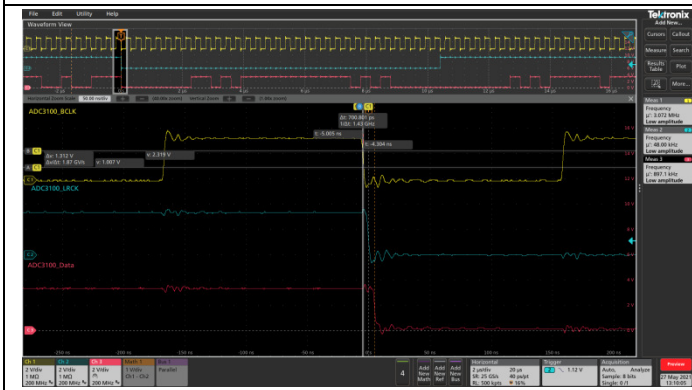


Figure 23: Fall time

Figure 24: TX_LRCK to TX_BCLK setup time

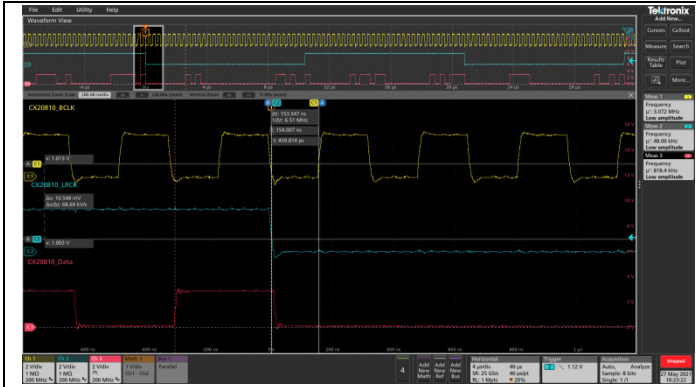


Figure 25: TX_LRCK to TX_BCLK hold time

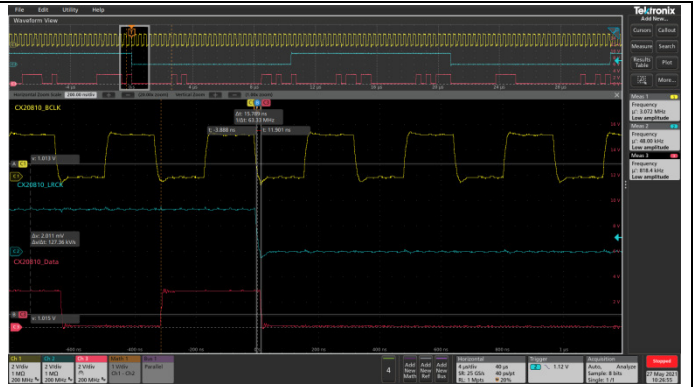


Figure 26: TX Data propagation delay from falling edge of BCLK